[11] P.D. Sulatycke and K. Ghose, "Caching Efficient Multithreaded Fast Multiplication of Sparse Matrices," *Proc. Merged Int'l Symp. Parallel Processing and Parallel and Distributed Processing,* pp. 117-124, 1998.
[12] M. Ujaldon, E.L. Zapata, S.D. Sharma, and J. Saltz, "Parallelization Techniques for Sparse Matrix Applications," *J. Parallel and Distributed Computing,* vol. 38, no. 2, pp. 256-266, Nov. 1996.
[13] M. Ujaldon, E.L. Zapata, B.M. Chapman, and H.P. Zima, "Vienna-Fortran/HPF Extensions for Sparse and Irregular Problems and Their Compilation," *IEEE Trans. Parallel and Distributed Systems,* vol. 8, no. 10, pp. 1068-1083, Oct. 1997.
[14] J.B. White and P. Sadayappan, "On Improving the Performance of Sparse Matrix-Vector Multiplication," *Proc. Int'l Conf. High Performance Computing,* pp. 711-725, 1997.
[15] E.L. Zapata, O. Plata, R. Asenjo, and G.P. Trabado, "Data-Parallel Support for Numerical Irregular Problems," *J. Parallel Computing,* vol. 25, nos. 13-14, pp. 1971-1944, 1999.
[16] L.H. Ziantz, C.C. Ozturan, and B.K. Szymanski, "Run-Time Optimization of Sparse Matrix-Vector Multiplication on SIMD Machines," *Proc. Int'l Conf. Parallel Architectures and Languages,* pp. 313-322, July 1994.

Zero-Aliasing Space Compaction of Test Responses Using a Single Periodic Output

Bhargab B. Bhattacharya, *Senior Member*, *IEEE*,
Alexej Dmitriev, and Michael Gössel

Abstract—A structure-independent method for space compaction in combinational circuits based on a new generic scheme is presented in this paper. It is shown that a single-output compactor can always be designed for compressing test responses of a circuit-under-test (CUT) with guaranteed zero-aliasing. Test responses from multiple outputs are compacted to a single periodic data stream. The compactor is independent of the fault model and can be designed only from the knowledge of the given test set and the corresponding fault-free responses. An additional response logic and a special code checker are used to design the compactor. The same test set given for the CUT also detects all multiple stuck-at faults in the response logic and almost all faults in the rest of the compactor. Further, time compaction is also easily achieved. Since the design can be accomplished without any information about the structure and functionality of the CUT, it would be useful for testing embedded cores as their internal structures may not be transparent to the users.

Index Terms—Space compaction, stuck-at faults, system-on-a-chip, testing.

1 Introduction

Space compaction of test responses is used to reduce the volume of test data at the outputs of a circuit-under-test (CUT). A typical response compaction scheme is shown in Fig. 1. The CUT is fed with n inputs $X = x_1, x_2, \ldots, x_n$ and its m outputs $y_1, y_2, \ldots, y_m$ are compacted by a space compactor to a q-bit data stream, $q \ll m$. The compaction ratio is defined as (m/q). For a single-output space compactor $(q = 1)$, the compaction ratio becomes maximum. Several techniques for designing space compactors are known, e.g., structure-independent methods [2], [12], structure-dependent methods [3], [4], [5], [6], and those based on coding theory [7], [8]. Other notable approaches appear in [9], [10]. For time compaction, mostly multioutput signature analyzers (MISA) are used. A major bottleneck in achieving high fault coverage under space compaction is aliasing, which renders a compacted faulty response indistinguishable from the fault-free response of the CUT. For coding technique-based approaches, 100 percent fault coverage and optimum space compaction cannot be guaranteed as the specific structure of the CUT is not considered. On the other hand, in all the previous structure-dependent methods, design of an efficient space compactor can only be accomplished by analyzing the response behavior of the CUT under the fault set, i.e., if the circuit structure and the fault model are known to the test engineer.

The use of embedded cores has emerged as a new paradigm in designing complex system-on-a-chip. However, its testing poses a new challenge [1]. Since an embedded core is often supplied as a black box, tools like ATPG, fault simulator cannot be run on the core. Therefore, the design of a suitable test response compactor for cores needs special techniques to ensure zero-aliasing with a high compaction ratio.

- B.B. Bhattacharya is with the ACM Unit, Indian Statistical Institute, Calcutta 700 108, India. E-mail: bhargab@isical.ac.in.
- A. Dmitriev and M. Gössel are with the Fault-Tolerant Computing Group, Institute of Computer Science, University of Potsdam, 14482 Potsdam, Germany. E-mail: {alexej, mgoessel}@cs.uni-potsdam.de.

Manuscript received 18 July 2000; revised 4 Oct. 2002; accepted 21 Mar. 2003.
For information on obtaining reprints of this article, please send e-mail to: tc@computer.org, and reference IEEECS Log Number 112543.

0018-9340/03/$17.00 © 2003 IEEE Published by the IEEE Computer Society