INDIAN STATISTICAL INSTITUTE

First-Semester Examination : 2025-26

Course Name: M. TECH. (QROR) I Yr.

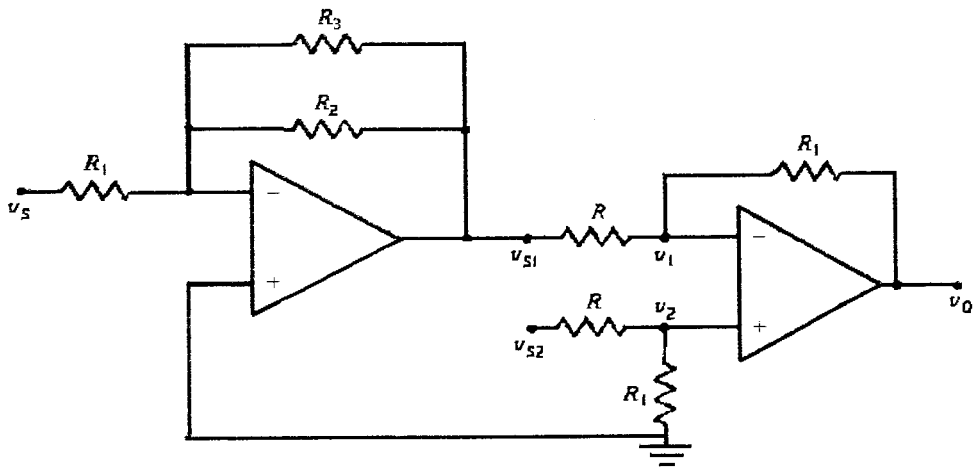
Subject Name : Electrical and Electronics Engineering

Date : 17.11.25 Maximum Marks : 96 Duration : 3Hrs

Answer any 6 questions.

1. a) Explain the operational principles of an OP-AMP to be used as an integrator.

b) For the circuit, given below, find the output voltage v_0 for v_{S1}=1volt, v_{S2}=0.5volt, R_1=2kOhm, R_2=8kOhm, R=2kOhm and R_3=8kOhm. [5+11=16]



2. a) Derive the output of a PID (proportional+ integral+ derivative) control action for a step type error signal. Explain with a figure how the output changes with error signal and time.

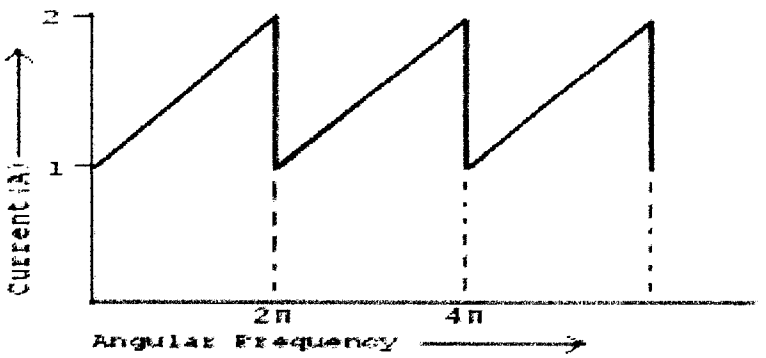
b) A PI (proportional+integral) controller is used for controlling a certain process. The settings are as follows: K_p (gain)=2%, P_b=40%, Reset rate =2%/min and E_p (error signal)=4t+6 where t represents time. What will be the controller output in percentage after 2 minutes? [(6+4)+6=16]

3. What is a transformer? Draw the equivalent circuit of a transformer and show that in ideal situation the ratio of the primary to the secondary voltage is equal to the primary-to-secondary turns ratio. [2+(3+11)=16]

4. State and prove Thevenin's theorem. [4+12=16]

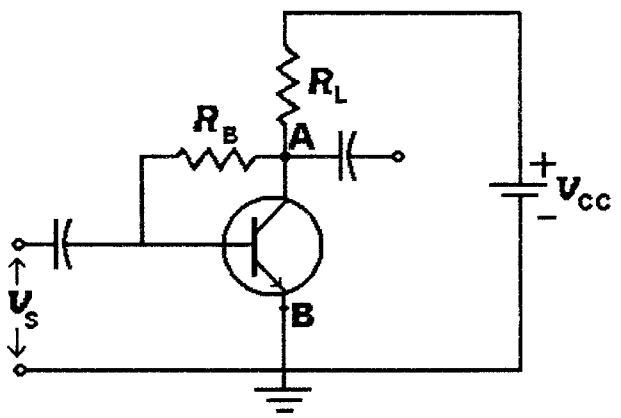
5. a) A DC voltage E is applied across a series RLC circuit. Find the steady state current in the circuit when $(R^2/4L^2)>(1/LC)$ and draw the respective curve of current w.r.t. time.

b) Calculate the average value of current represented in the figure below. [(8+2)+6=16]



6. a) Draw and explain the circuit diagrams of amplifiers using a p-n-p transistor in common-base and common-emitter modes of operation.

b) An n-p-n transistor, shown in the figure below, is used in common-emitter amplifier mode with β=49, V_{cc}=10V and R_L=2k Ohm. If a 100k Ohm resistor, R_B, is connected between the collector and the base of the transistor, then calculate the collector to emitter voltage drop between points A and B. Assume V_S=0V. [(4+4)+8=16]



7. a) How a D flip-flop and a T flip-flop can be designed using JK flip-flops?

b) Explain the operation of a 4 bit shift register with circuit diagram and time table to input binary data 1011. [(3+3)+10=16]

8. a) Derive the binary equivalent of 75.25.

b) Subtract 01001 from 10011 using 2's complement method and verify the result by doing the same subtraction using 1's complement method.

c) Show how an AND gate can be realized using diodes and resistances.

d) Construct an OR gate with AND and NOT gates only.

[2+6+3+3=16]