INDIAN STATISTICAL INSTITUTE

End-semester Examination: 2025-2026

Course Name : M.TECH. (CS)

Subject name : COMPUTER ORGANIZATION

Date : November 18, 2025   Maximum Marks : 50   Duration : 3 hours

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Answer any 5 questions. Notations are as used in the class.

1. (a) Design a synchronous counter using JK flip flops, that generates the outputs in the order 000, 011, 101, 100, 111, 010, 001, 110 and 000. [6]

   (b) Present the design of an encoder where a keyboard uses 10 keys corresponding to the numbers 0, 1, 2, $\cdots$ 9 as input lines and 4 bits to produce outputs. [4]

2. (a) 9's complement of a decimal number is the result obtained by subtraction of each of its digits from 9. Like 1's complement, we can use 9's complement for subtraction using addition. Using this idea, compute 718 - 123 using 9's complement and addition. Explain the steps involved. [6]

   (b) What are the conditions for detecting an overflow while adding two 2's complement numbers? [4]

3. (a) Use the Booth algorithm to multiply 25 (multiplicand) by -13 (multiplier), where each number is represented using 16 bits. [6]

   (b) Present a simple strategy to compare two 32 bit IEEE-754 floating point numbers. You do not need to consider $\pm$inf, NAN, and negative 0. What is the time complexity of your algorithm in terms of the sizes of the operands? [4]

4. (a) Present a data-path diagram for a circuit that performs restoring division with 2 n-bit numbers. [6]

   (b) Consider a load instruction using the Immediate Addressing mode and another load using the PC-Relative Addressing mode. Which is expected to execute faster? Justify your answer. [2]

   (c) Consider the jump instruction j-immediate that has a 26-bit immediate value specified as part of the instruction itself. For a jump instruction, the next 32-bit address to be loaded into the Program Counter (PC) after the jump is executed, is computed as below, by concatenating the top 4 bits of the current PC (after incrementing by 4) with the 26-bit immediate left shifted by 2 bits, as specified below.

   ```
   target = {PC[31:28], immediate26, 2'b00 }
   PC = target
   ```

   Can a j-immediate instruction be such that its own address becomes the target address loaded into the PC for the next cycle? Explain your answer. [2]

5. Consider a 6-stage pipelined inorder processor with separate data and instruction memory, and a dual port register file. The pipeline stages are IF (Instruction Fetch), ID (Instruction Decode), RR (Register Read), EX (Execution / Address Computation), MEM (Memory Access) and RWB (Register Write Back). Every instruction has to go through all stages of the pipe. All stages (except EX) take 1 processor clock cycle. The EX stage takes different clock cycles depending on the instruction as given below.

Operation	Clock Cycles
MUL	2
DIV	3
ADD	1
SUB	1
LOAD	1

MUL	R2,R0,R1	#R2 $\leftarrow$ R0 * R1
DIV	R5,R3,R4	#R5 $\leftarrow$ R3 / R4
LOAD	R1,10[R5]	#R1 $\leftarrow$ MEM[R5 + 10]
ADD	R6,R1,R7	#R6 $\leftarrow$ R1 + R7
SUB	R8,R3,R4	#R8 $\leftarrow$ R3 - R4

(a) Draw the pipeline execution diagram for the above code that *minimises* the number of clock cycles needed, assuming that operand forwarding between stages is available, but no instruction reordering is permitted. You may insert as many $STALL$ cycles as necessary to ensure correct execution. Also, clearly mark the stages between which forwarding needs to be set up, if at all. [6]

(b) Recompute the *minimum number* of clock cycles, assuming that *instruction reordering* is permitted, provided the final output remains correct. [4]

6. (a) Assume that the delay of all basic gates (AND, OR, NAND, NOR, NOT) is δ. Consider the design of a Full Adder using basic gates. Derive the expression for the Carry Delay and Sum Delay. [2]

(b) An n-bit Ripple Carry Adder (RCA) is built with a cascade of n full adders. Derive the expression for the delay in the final sum and carry for a RCA. [5]

(c) Consider an architecture that supports numbers in base 3 instead of base 2. Design a Carry Look-ahead adder (CLA) for this system. Assume you have a simple full-adder which adds 2 numbers in base 3. [3]

7. (a) You are given a processor having a single-level cache hierarchy with only an L1 cache that has a 95% hit rate and main memory as usual. You have to re-design the cache hierarchy without increasing the Effective Memory Access Time (EMAT), using a smaller and cheaper L1 cache with a lower hit rate of 0.9, and an L2 cache along with the main memory. Show that the access time of the L2 cache should be no greater than 1/2 that of the main memory. [6]

(b) Compare and contrast SRAM and DRAM with respect to the following parameters:

(i) Access Time

(ii) Number of Transistors required to store a bit [2 + 2]

8. (a) Consider the following information about a magnetic hard disk, with cylinders numbered 0 (innermost) to 511 (outermost):

- at time $t = 0$ ms, the disk head is at cylinder **120**, moving outwards towards cylinder 511;
- the disk arm takes **1** ms to seek from cylinder i to cylinder $i + 1$ or cylinder $i - 1$;
- the time taken to read sectors from a single cylinder may be neglected.

The following sequence of I/O requests arrive at the disk controller.

Request no.	**Arrival time (ms)**	**Cylinder no.**
r_1	1	480
r_2	10	240
r_3	15	360
r_4	20	100
r_5	25	140
r_6	30	185

Compute the total number of head movements if the six requests are serviced by the controller using a **preemptive** SHORTEST SEEK TIME FIRST (SSTF), approach i.e., the scheduling algorithm is run whenever a new I/O request arrives, thus the disk head while moving towards a particular cylinder request may decide to change its direction if a shorter seek time (with respect to its current position) request arrives towards the other end (opposite to its current movement). [8]

(b) Define rotational latency in the context of a disk. [2]