INDIAN STATISTICAL INSTITUTE

Mid-Semester Examination : 2025-26 (First Semester)

Course Name: M. TECH. (CS) I Yr.

Subject Name : Computer Organization

Date: 10.09.25 Maximum Marks: 40 Duration: 2 Hrs

Answer any 4 questions.

1. a) Draw the circuit diagram of a JK flip-flop and explain its operation with a truth table.
   b) How a T flip-flop can be designed using JK flip-flop? [(2+6)+2=10]

2. a) Implement the Boolean function $Y = AB + \overline{A}C$ with NOR gates only.
   b) Subtract 11110 from 10011 using 1's complement method.
   c) Prove or disprove (with a counterexample) the statement: The minimal sum-of-products of any Boolean function is always the sum of all the prime implicants of the function. [3+2+5=10]

3. a) Design the circuit of an EXCLUSIVE-NOR gate with a truth table.
   b) Explain the operation of a full adder with circuit diagram and truth table. [(2+1)+(5+2)=10]

4. a) Derive the octal equivalent of the decimal number 75.25
   b) Show that an OR gate can be realized with diodes, batteries and resistances.
   c) Simplify the function $Y= \overline{A}BC + A\overline{B}C + AB\overline{C} + ABC$ by using a Karnaugh map. [2+5+3=10]

5. Consider a serial (one bit per cycle) two's complementer circuit with 2 inputs, Start and X, and one output Q that is the two's complement of the input X. A binary number of arbitrary length is provided at input X, one bit per cycle, starting with the least significant bit from the first cycle. The corresponding bit of the output appears at Q bit by bit, starting from the first cycle. For example, if the complementer circuit is given the 8-bit input X = 00000110 over 8 cycles (with the LSB 0 input in the first and the remaining bits over the next 7 cycles), it should produce the output 11111010 on Q over 8 cycles, starting with the LSB 0 in the first cycle and the remaining bits over the next 7 cycles. Similarly, for the 4-bit input 1110 (with the LSB 0 input in the first cycle), it should produce the output 0010 on Q, starting with the LSB 0 in the first cycle.

   a) Design a Finite State Machine (FSM) for the above circuit.
   b) Using binary state encoding, complete a state transition table and output table for the FSM.
   c) Using a suitable choice of flip-flops, present a schematic circuit description. [(3+5)+2=10]